REMARKS

Claims 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano et al. (US 6,445,011) in view of Tominaga (US 2002/0008325). Applicants have amended claim 7 to more clearly define the present invention and respectfully traverses the rejections for the reasons given below:

Claim 7 partly defines:

a light-emitting diode package structure, comprising:

a semiconductor sub-mount having a first surface with a cavity therein;

a first patterned conductive-reflective film set up on a portion of the first surface, a first sidewall of the cavity and a bottom surface of the cavity, wherein the first patterned conductive-reflective film substantially covers the first sidewall of the cavity;

a second patterned conductive-reflective film set up on a portion of the first surface, a second sidewall of the cavity and a bottom surface of the cavity, wherein the second patterned conductive-reflective film substantially covers the second sidewall of the cavity; and

a light-emitting diode chip set up inside the cavity of the semiconductor sub-mount.....

In the Office Action, Examiner admits that Hirano does not teach that a first patterned conductive-reflective film set up on a portion of the first surface, a first sidewall of the cavity and

a bottom surface of the cavity; and a second patterned conductive-reflective film set up on a portion of the first surface, a second sidewall of the cavity and a bottom surface of the cavity. Examiner contended that Tominaga shows a light emitting diode package structure having silicon sub mount 11 having a first surface including a cavity including a bottom surface, a first sidewall and a second sidewall wherein a first conductor 13 is set up on a portion of the first surface, bottom surface and first sidewall, a second conductor 13 is set up on a portion of the first surface and a second sidewall.

However, Tominaga only discloses a wiring layer 13 formed in the recess 12, continuously extending from the bottom 12a to the top surface via the side 12b of the recess 12.(Col. 2, par. [0033]) In Tominaga, the function of the wiring layer 13 is to electrically connect the terminal pads located on the surface of the semiconductor chip 14 with an external electric component located at the top surface of the base 10. Tominaga keeps silent about whether the wiring layer 13 is reflective. As such, Tominaga fails to disclose a first patterned conductive-reflective film set up on a portion of the first surface, a first sidewall of the cavity and a bottom surface of the cavity, ***wherein the first patterned conductive-reflective film substantially covers the first sidewall of the cavity***; and a second patterned conductive-reflective film set up on a portion of the first surface, a second sidewall of the cavity and a bottom surface of the cavity, ***wherein the second patterned conductive-reflective film substantially covers the second sidewall of the cavity.***

Accordingly, Hirano discloses the electrodes 422, 422 are formed directly under the chip 100, and fails to teach the substrate has a cavity and the side surfaces of the cavity are covered by

a conductive-reflective film. Tominaga does not teach whether the wiring layer 13 is reflective and also fails to teach the side surfaces of the cavity 12 are covered by reflective film. Therefore, neither Hirano nor Tominaga discloses a first patterned conductive-reflective film set up on a portion of the first surface, a first sidewall of the cavity and a bottom surface of the cavity, wherein the first patterned conductive-reflective film substantially covers the first sidewall of the cavity; and a second patterned conductive-reflective film set up on a portion of the first surface, a second sidewall of the cavity and a bottom surface of the cavity wherein the second patterned conductive-reflective film substantially covers the second sidewall of the cavity.

Moreover, as expressly described in Hirano, the negative electrode 421 and the positive electrode 422, both formed of aluminum, together are formed over the **entirety** of the insulation film on the semiconductor substrate serving as the sub-mount, the negative electrode 421 and the positive electrode 422 constitute a reflection surface. (Col. 11, lines 47-52) However, in Tominaga, as alleged by the name and shown in FIGS. 8A-12, the wiring layer 13 is wire-shaped and only **partly** covers the base 10. As such, combination of Hirano and Tominaga would render Hirano unsatisfactory for its intended purpose. Therefore, there is no suggestion/motivation to combine Hirano and Tominaga.

Accordingly, claim 7 should be patentable over Hirano in view of Tominaga. Reconsideration and withdrawal of the rejection and allowance of claim 7 is respectively requested.

Claims 8-15 should also be patentable since they depend on allowable claim 7 directly or indirectly.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 7-15 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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